KU LEUVEN

# Integrated SC DC-DC Converters for Energy Storage Applications

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## Outline

- **Introduction**
- Switched-Capacitor Converters
- Improvements for Energy Storage
- Design Example
- Conclusions

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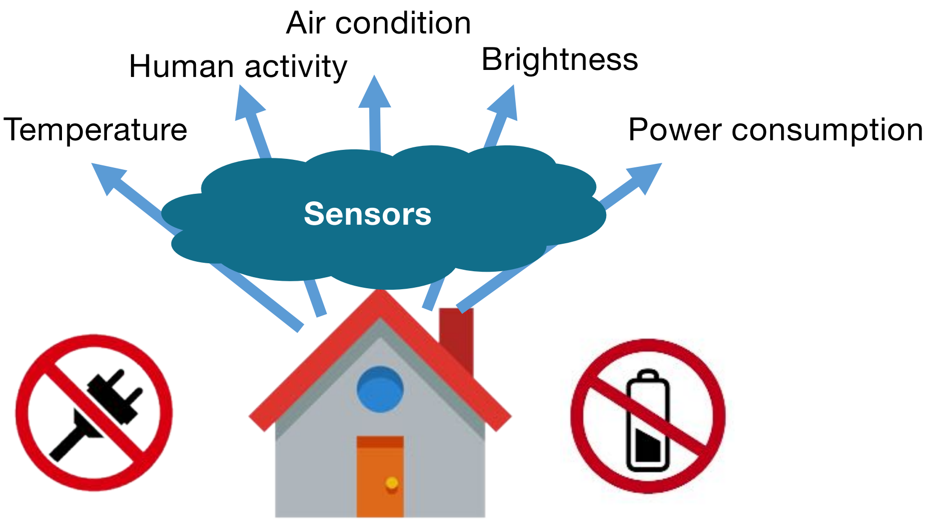
# Wireless Sensor Nodes

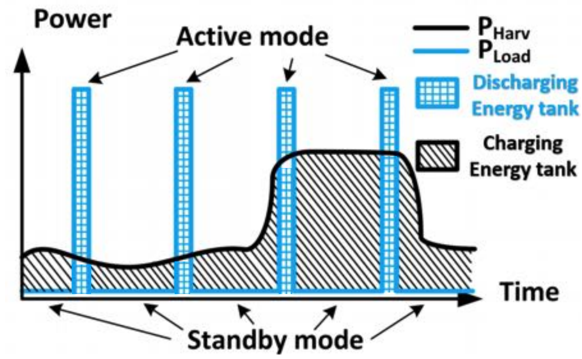





# Energy Harvesting

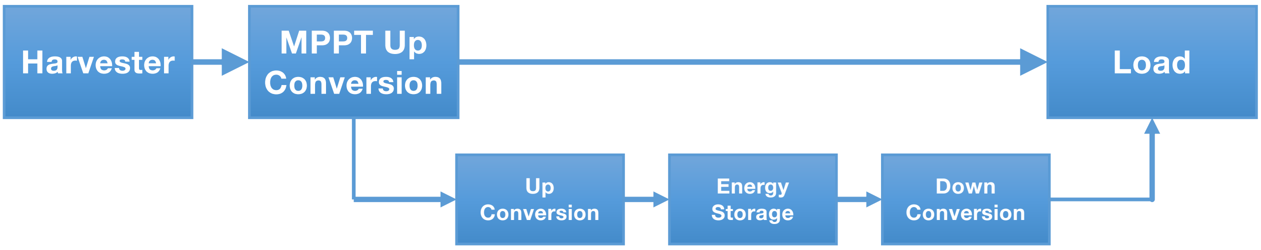
# Energy Flow


- Small duty cycle
- $P_{harvester} \ll P_{load}$
- All power converted twice

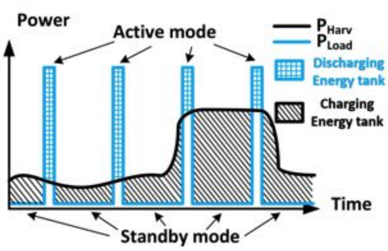



[1,2] 5

# Alternative Energy Flow




- Direct path to load
- Maximum Power Point Tracking (MPPT)
- Only excess power converted twice




[1,3,4] 6

# Energy Storage Possibilities

Harvester 10(0)'s mV → Up Conversion → Energy Storage → Down Conversion → Load ~ 1 V

'Fixed' $V_{storage}$

$V_{storage} > V_{load}$

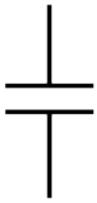
High Conversion Step

[1, 4]

$E \sim CV^2 \rightarrow$ Variable $V_{storage}$

$V_{storage} \geq V_{load}$

Wide Conversion Range



[3, 5]

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  - **General behaviour**
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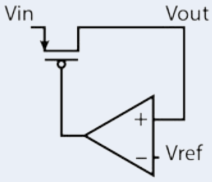
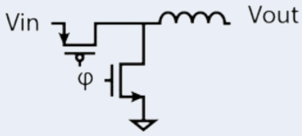
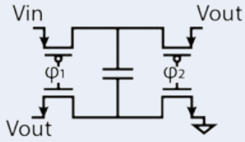
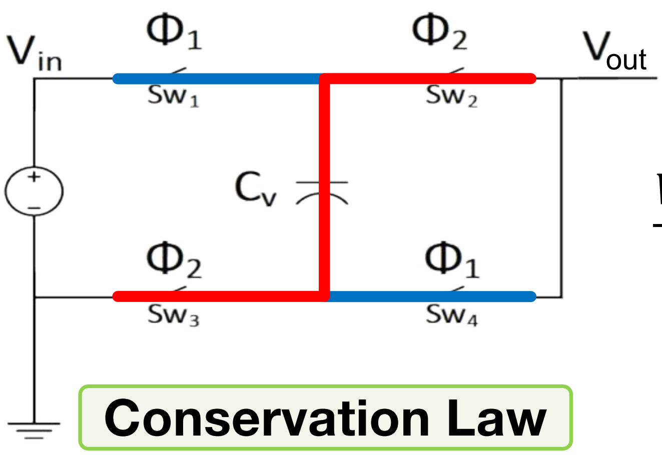
# Converting Voltages

| | LDO | Switched-Inductor | Switched-Capacitor |
|---|---|---|---|
| Energy Transfer | Resistor | Inductor | Capacitor |
| Direction | Only Step-Down | Step-Up & Step-Down | Step-Up & Step-Down |
| $\eta_{max}$ | $\frac{V_{out}}{V_{in}}$ | 1 | $\frac{V_{out}}{iVCR * V_{in}}$ |
| Circuit |   |   |   |



# Principle of SC Converters

$$Q_{\Phi 1} = C_v * (V_{in} - V_{out}) \qquad Q_{\Phi 2} = C_v * (V_{out} - 0)$$

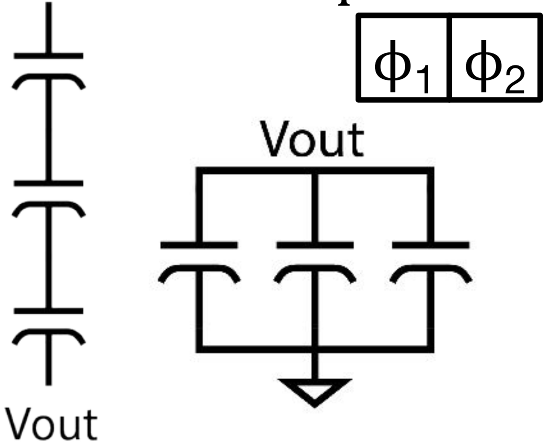



$$\frac{V_{out}}{V_{in}} = \frac{1}{2} = iVCR$$

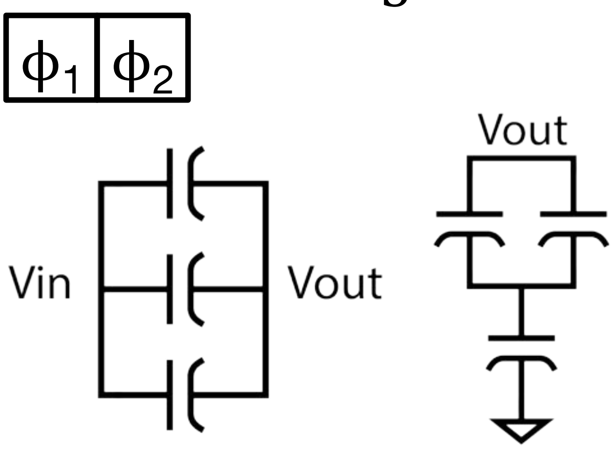
**Conservation Law**

# Other Ratios = Other Topologies

$iVCR = \frac{1}{4}$




$iVCR = \frac{2}{3}$



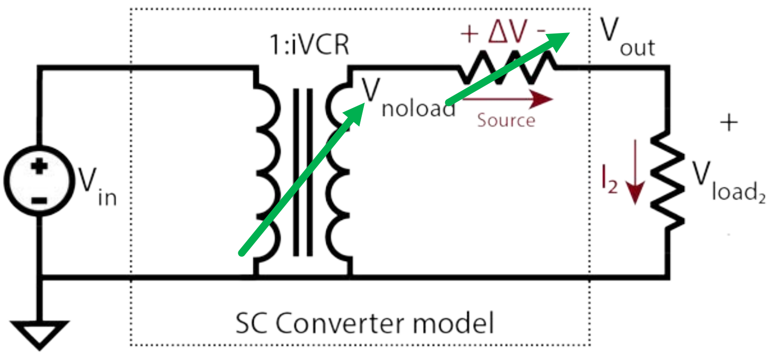



# Modelling SC Converters

iVCR = f(topology)

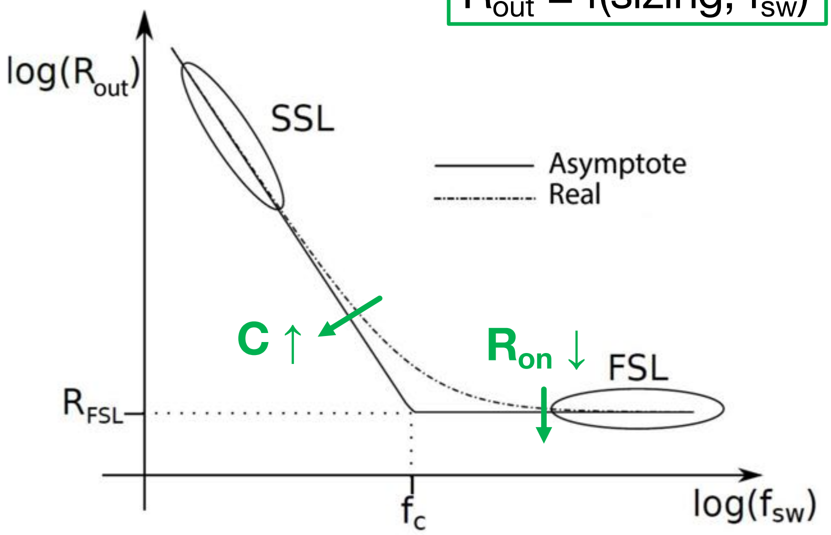
$R_{out}$ = f(sizing, $f_{sw}$)

$$V_{out} = V_{in} * VCR$$
$$V_{noload} = V_{in} * iVCR$$
$$V_{out} = V_{noload} - R_{out} * I_{load}$$



# $R_{out}$ Behaviour

$R_{out} = f(\text{sizing}, f_{sw})$




- $f_{sw}$:
  - SSL: Slow-Switching Limit
  - FSL: Fast-Switching Limit
- sizing:
  - $R_{on}$: depends on switch size
  - C: defines charge per clock cycle in SSL

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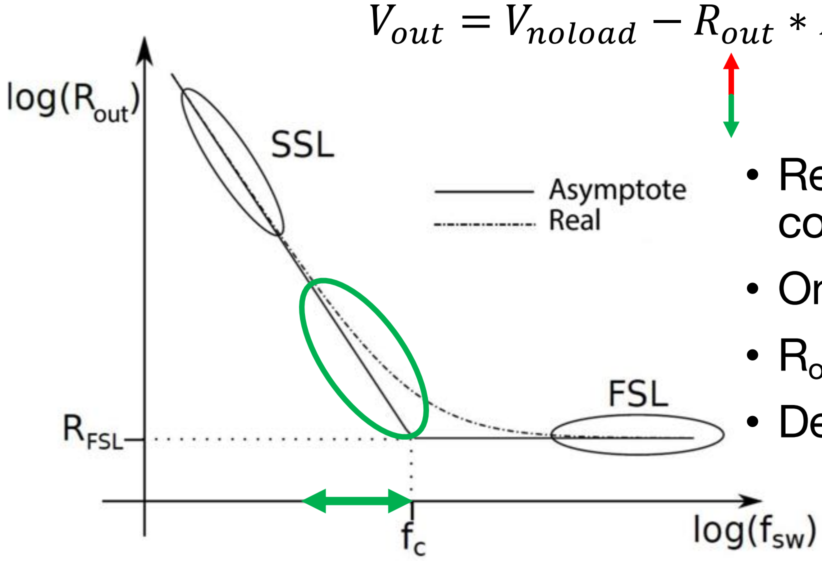
# Regulating SC Converters

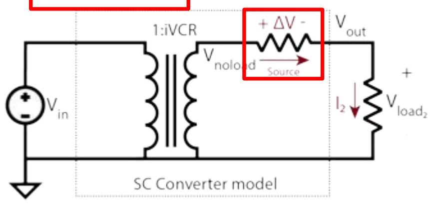
$$V_{out} = V_{noload} - R_{out} * I_{load}$$




- Regulation = keep $V_{out}$ constant
- Only $f_{sw}$ can be changed
- $R_{out}$ results in losses
- Design close to $f_c$

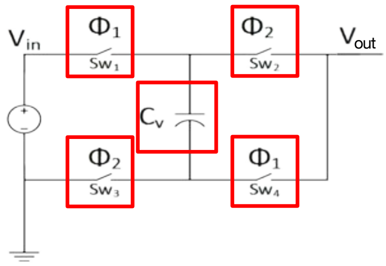
# SC Converter Losses

$$P_{loss} = I_{load}^2 * R_{out} + P_{par,switch} + P_{par,cap}$$




$$P_{par,switch} = f_{sw} * \sum_i C_{gate,i} * V_{gs,i}{}^2$$

$$P_{par,cap} = f_{sw} * \sum_i C_{bp,i} * \Delta V_{bp,i}{}^2$$

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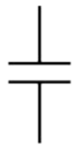
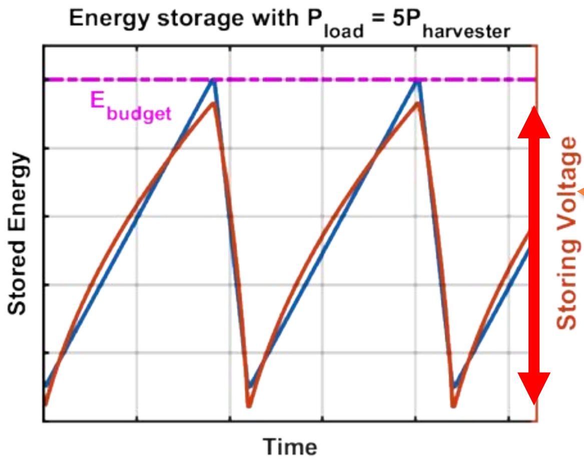
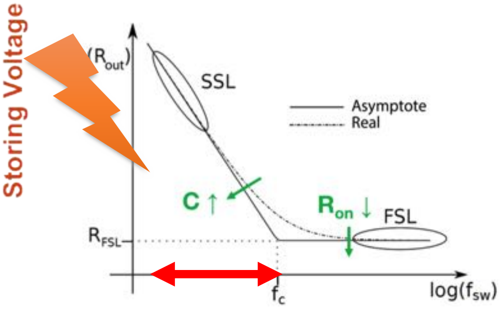
# Why Wide-Range Converters?



$E \propto CV^2$




$P_{loss} \sim I_{load}^2 * R_{out}$




**Wide-range at the expense of high losses**

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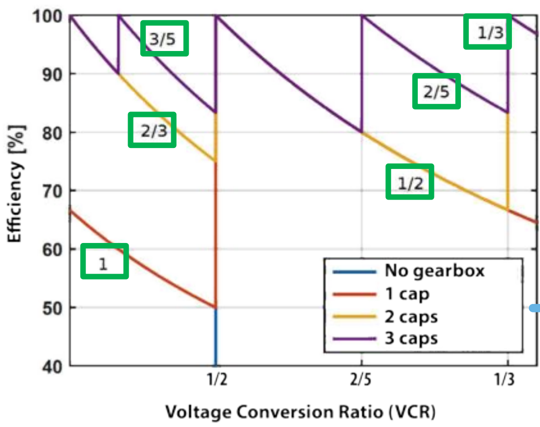
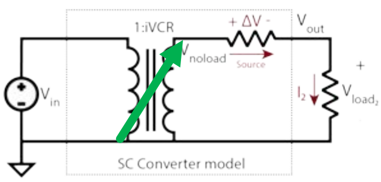
# Gearbox = Change Topology

iVCR = f(topology)

$V_{noload} = V_{in} * iVCR$

$V_{out} = V_{noload} - R_{out} * I_{load}$




Fibonacci:
1, 2, 3, 5, 8, 13, …

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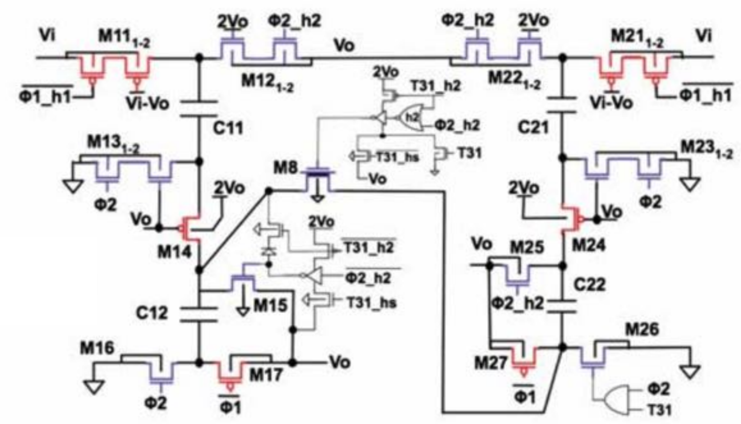
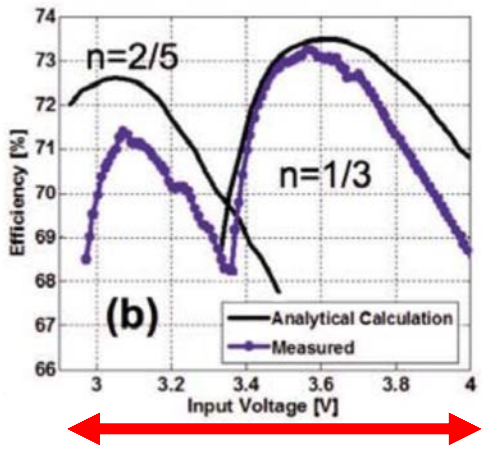
# Gearbox Converters – Example 1




**Complex and lower peak efficiency**

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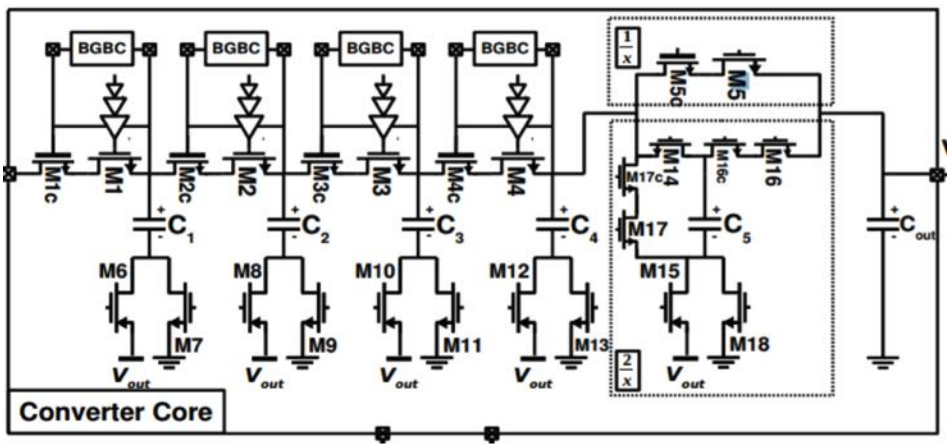
# Gearbox Converters – Example 2




**Complex**

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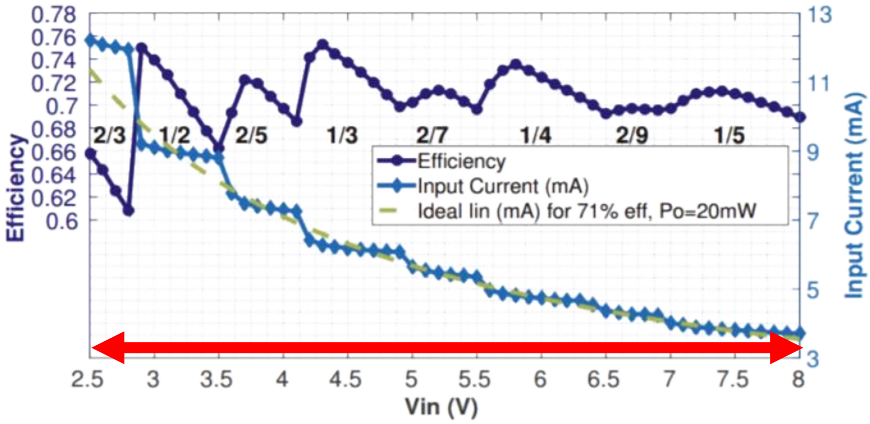
# Gearbox Converters – Example 2

**Higher average efficiency**




**Complex and lower peak efficiency**

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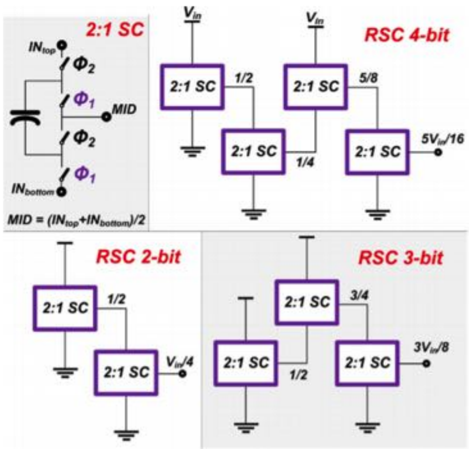
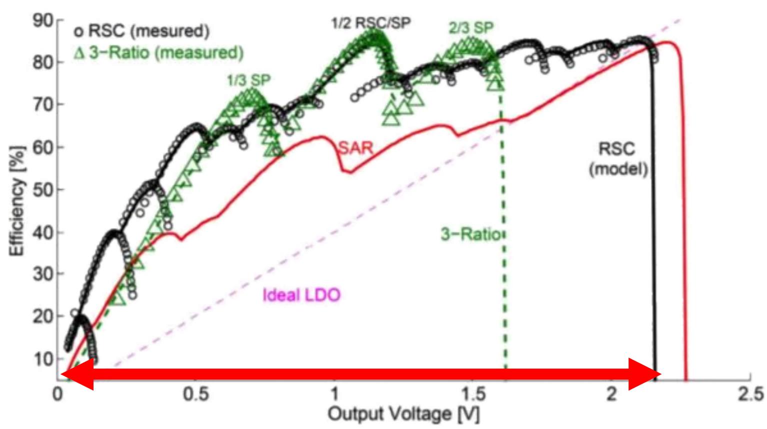
# Gearbox Converters – Example 3




**Complex and lower peak efficiency**

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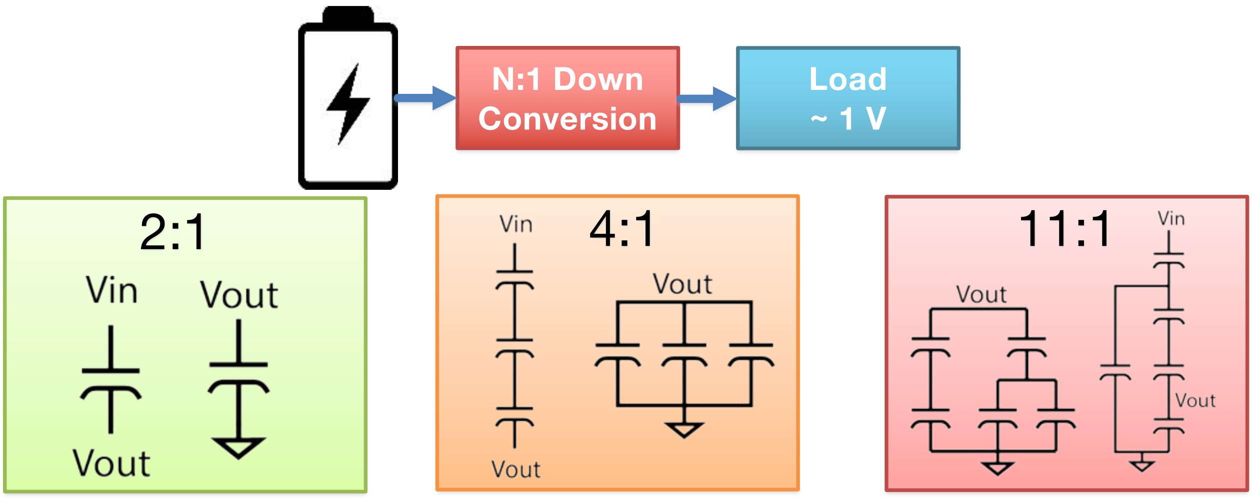
# High-Step Conversion




**High-step results in many capacitors**

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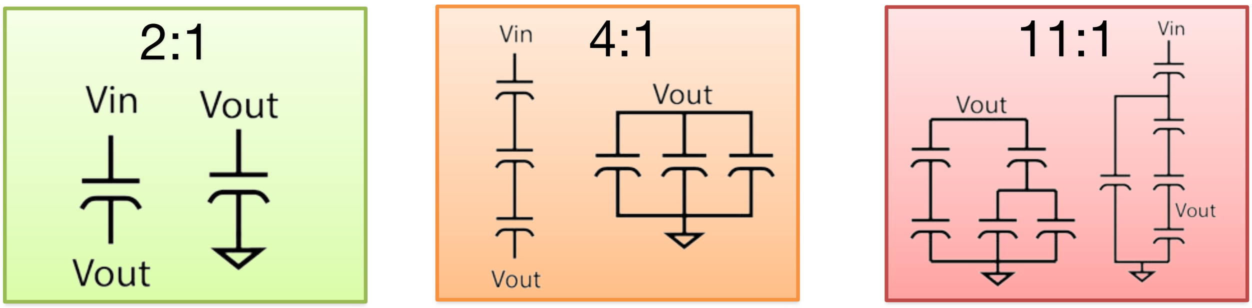
# Efficiency of Capacitance Usage

$$K_c \geq \frac{(N-1)^2}{N^2}$$

$$\frac{\mathbf{1}}{\mathbf{4}} \rightarrow \frac{4}{9} \rightarrow \frac{\mathbf{9}}{\mathbf{16}} \rightarrow \dots \rightarrow \frac{\mathbf{100}}{\mathbf{121}}$$




**High-step results in large $K_c$**

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# What now?

- SC DC-DC Conversion for Monolithic Integration
- Wide-Range for Capacitive Storage
- High-Step for Battery and Capacitive Storage

**Can we change the architecture to ease the converter requirements and limit the losses?**

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  - Dynamic Voltage Scaling (DVS)
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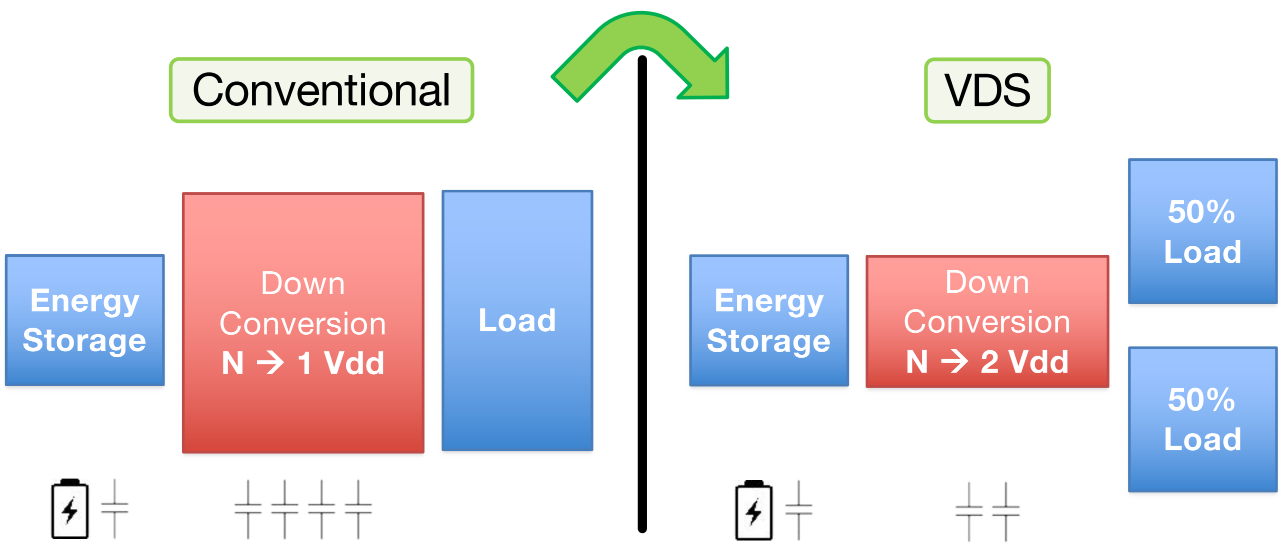
# Voltage Domain Stacking (VDS)

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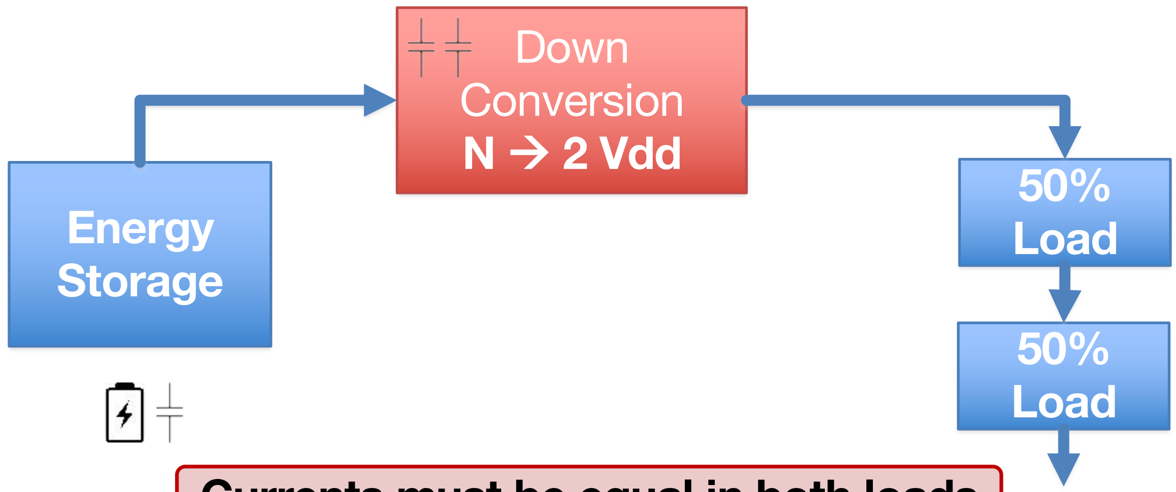
# Load Matching




Currents must be equal in both loads

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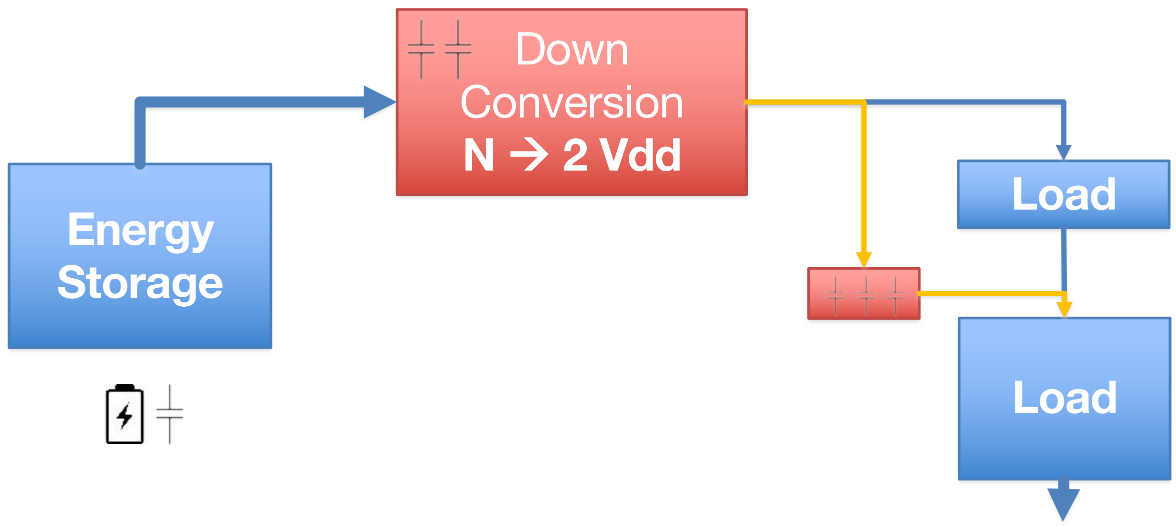
# Unequal Load Currents - Source

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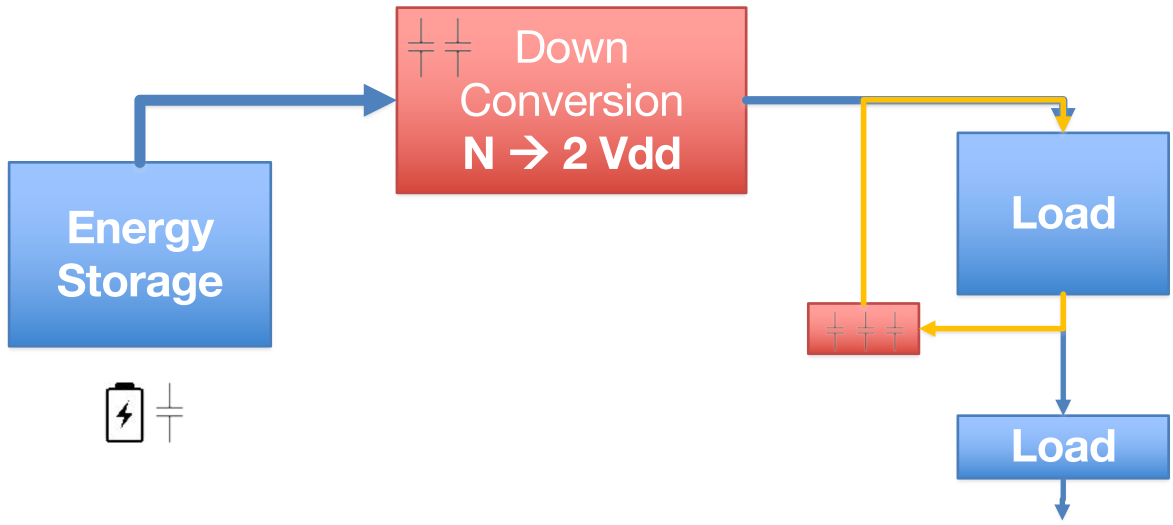
# Unequal Load Currents - Sink

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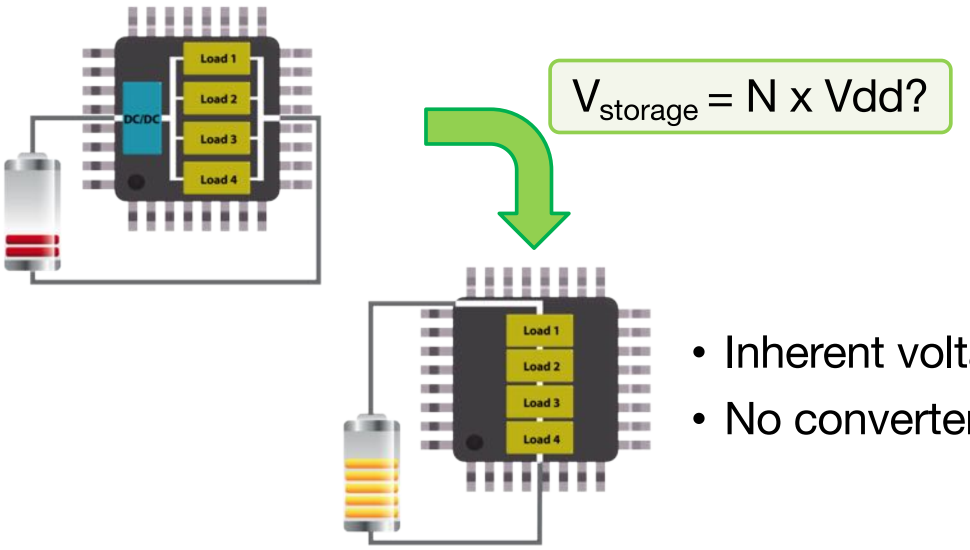
# The Ideal Scenario




- Inherent voltage division
- No converter losses!

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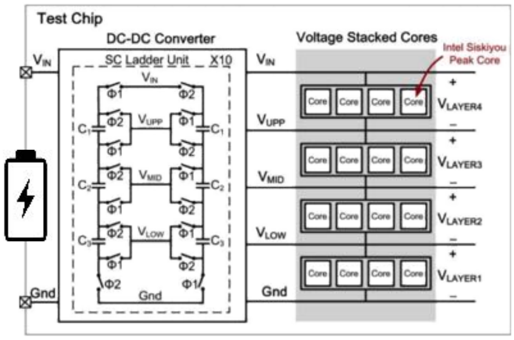
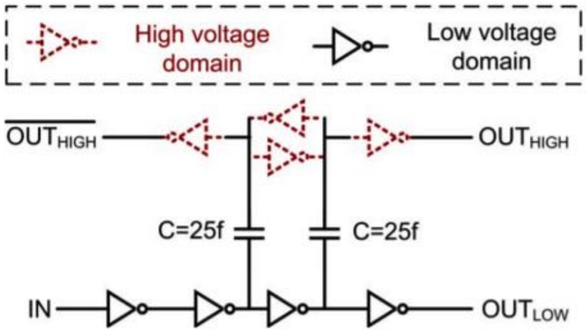
# VDS Example

- Only unbalance currents converted → **Losses** ↓↓
- Interlayer communication → Level Shifters

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  - **Dynamic Voltage Scaling (DVS)**
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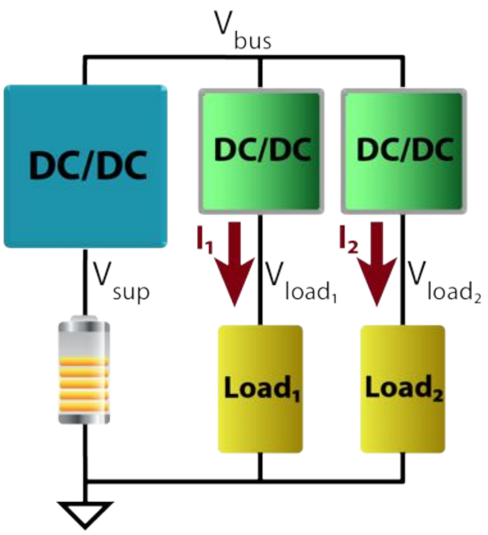
# Dynamic Voltage Scaling (DVS)




Functional blocks

- Significant power reduction if speed in load is low
  → **reduce supply voltage**
- Highly loaded converters
  → **large area**
  → **high losses**

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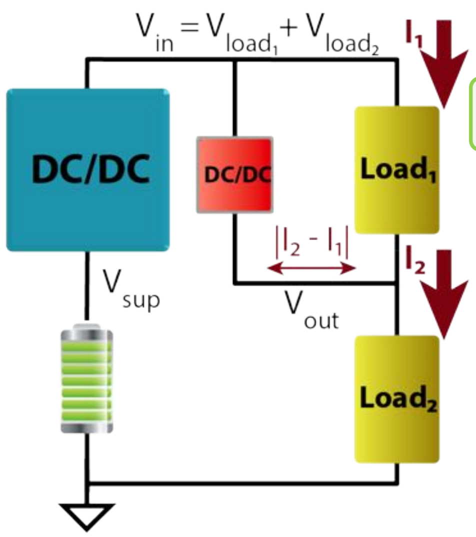
# VDS Meets DVS




DC-DC + functional blocks

- Lowly loaded converter
  → **small area**
  → **low losses**
- Wide Range ($V_{in}$, $V_{out}$)
- Two load directions

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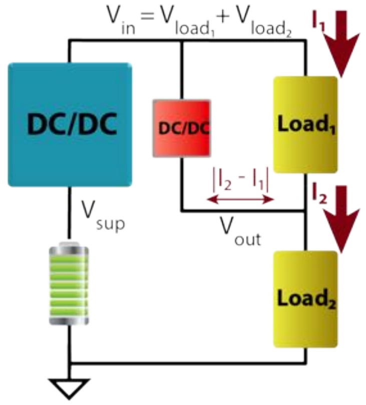
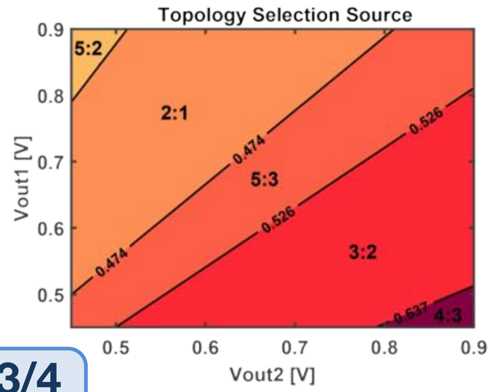
# Wide Range Requirements

$$V_{load} = [0.45V \ ... \ 0.9V]$$

$$VCR = \frac{V_{out}}{V_{in}} = \frac{V_{load_2}}{V_{load_1} + V_{load_2}} = 1/3 \rightarrow 2/3$$




**5 iVCR's: 2/5 → 3/4**

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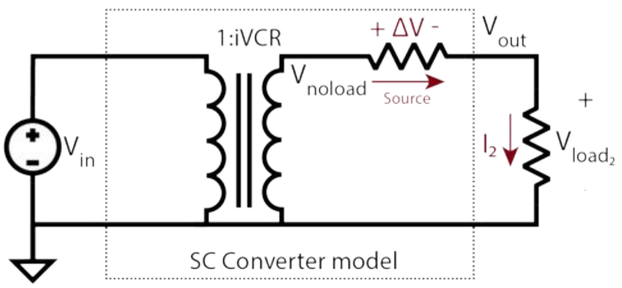
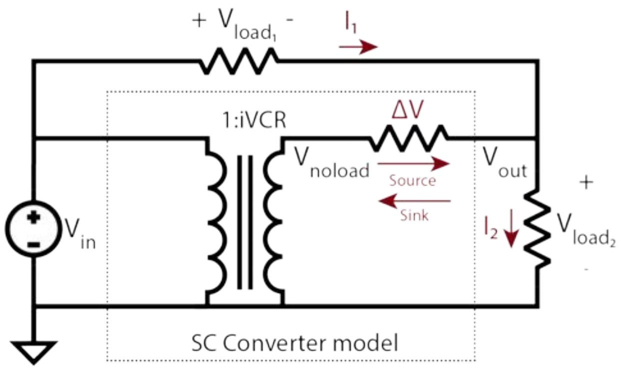
# Load Stacking Implications

**Conventional** | **VDS**




- Always source
- iVCR = f(VCR)




- Sink and Source
- iVCR = f(VCR, direction)

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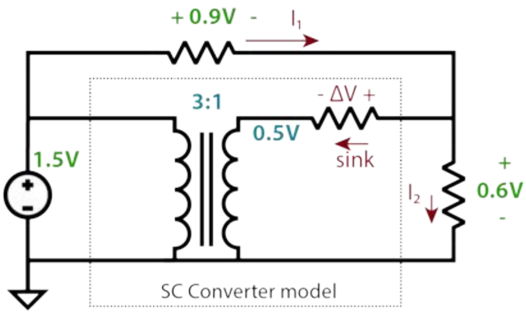
# Load Stacking Implications

Sink

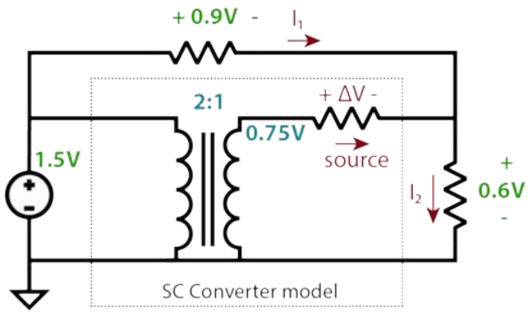
$$VCR = \frac{V_{load_2}}{V_{load_1} + V_{load_2}} = 0.4$$

Source

$VCR > iVCR = 1/3$




$VCR < iVCR = 1/2$

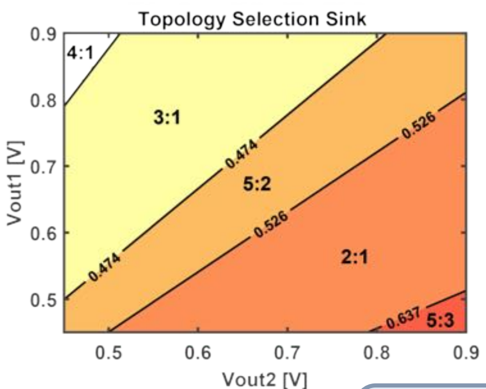



**1 VCR → 2 iVCR's**

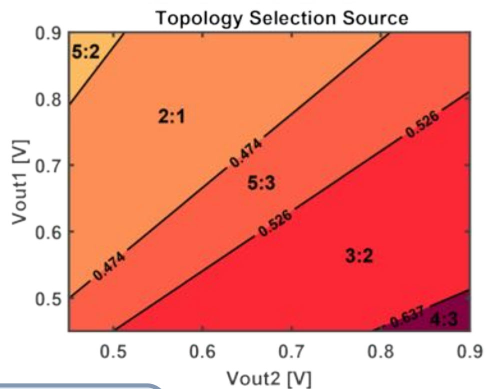


# Wide Range and Load Stacking

$VCR > iVCR$




$VCR < iVCR$




**7 iVCR's: 1/4 → 3/4**

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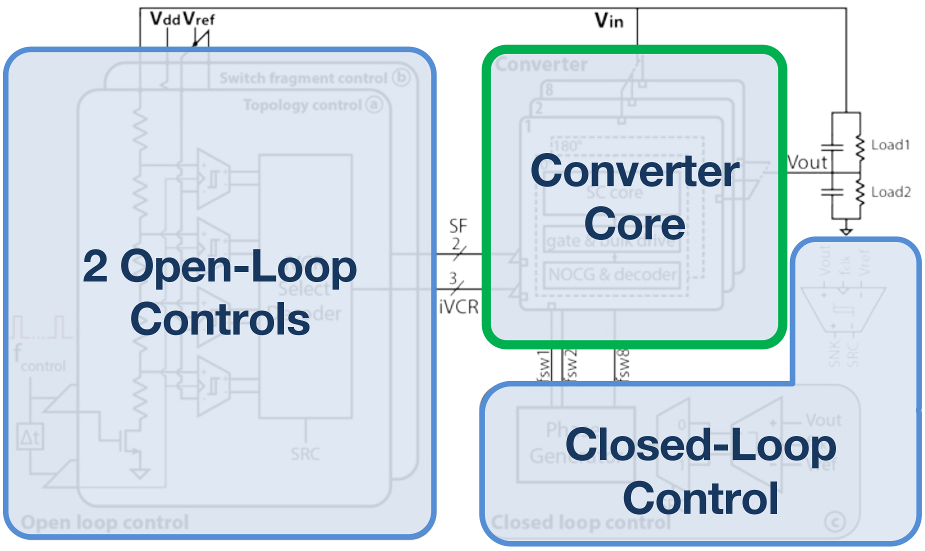
# Toplevel Architecture

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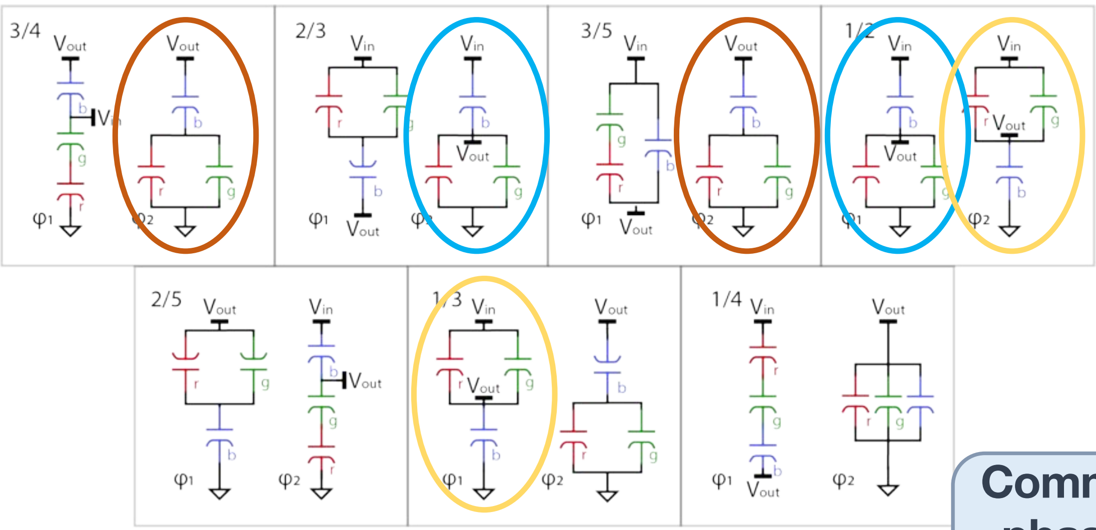
# Gearbox SC Core - Topologies




Common phases

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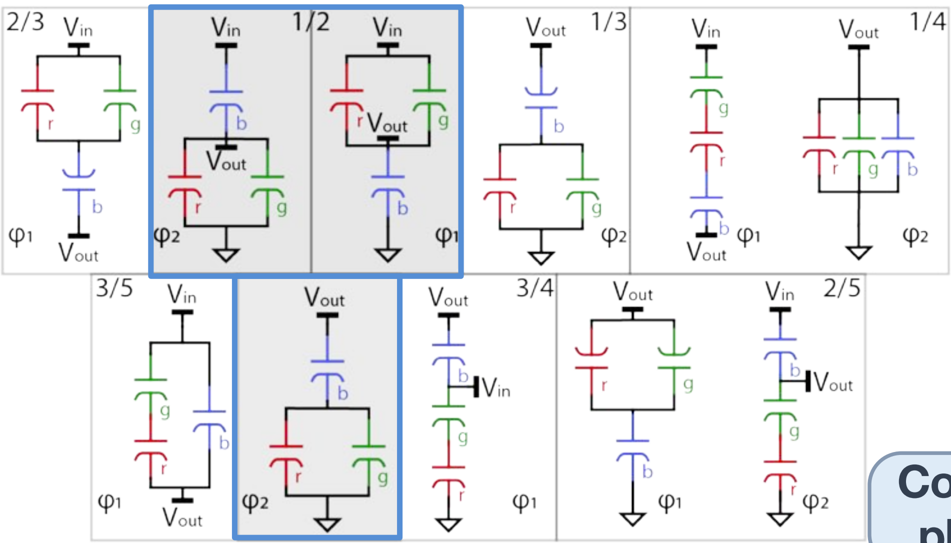


Common phases

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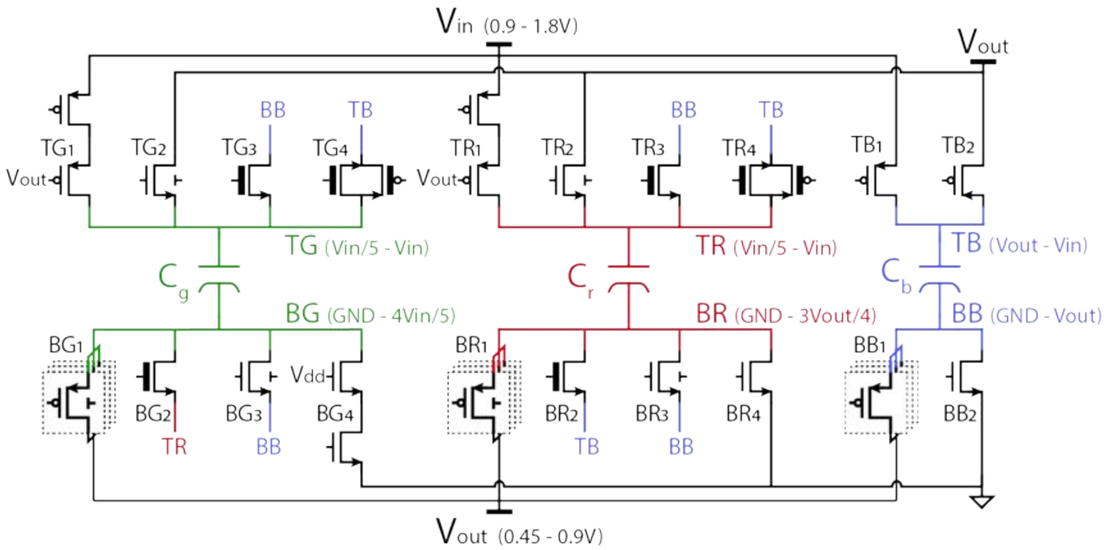
# Gearbox SC Core

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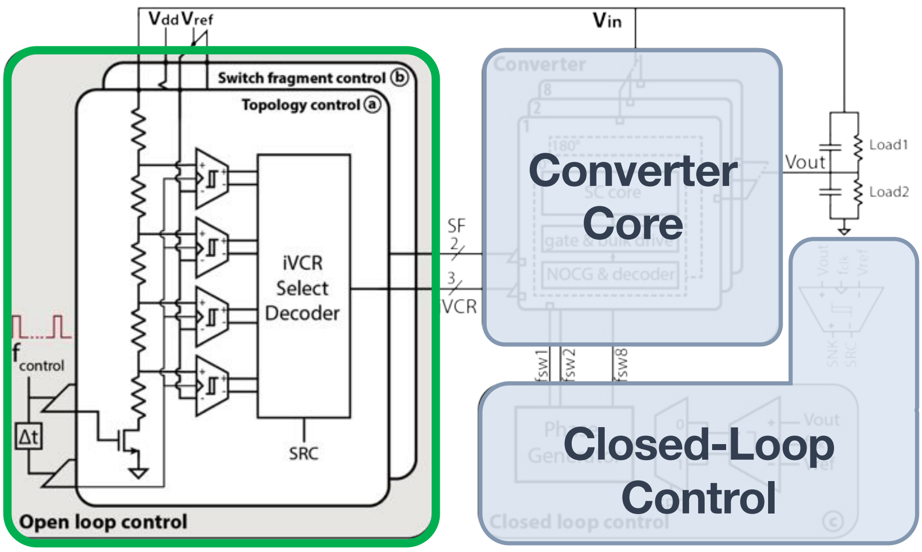
# Toplevel Architecture

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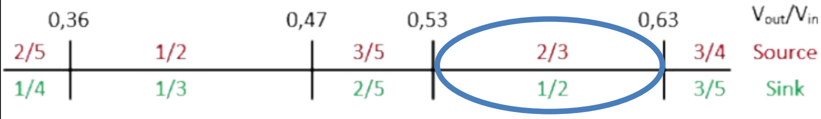
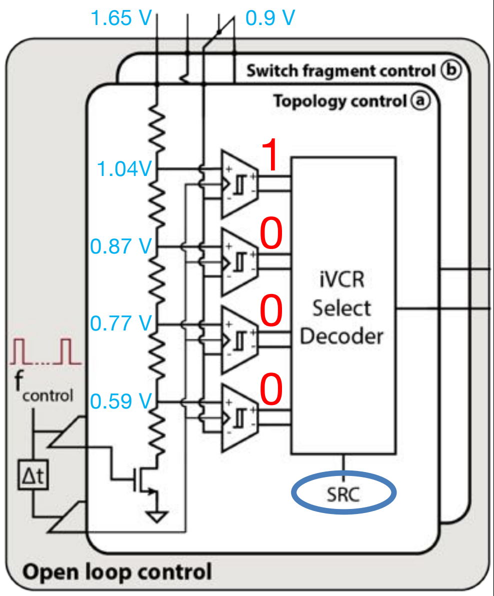
# 2 Open-Loop Controls

- $V_{load1}$ = 0.75 V
- $V_{load2}$ = 0.9 V
- VCR = 0.54




| | | | | |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |

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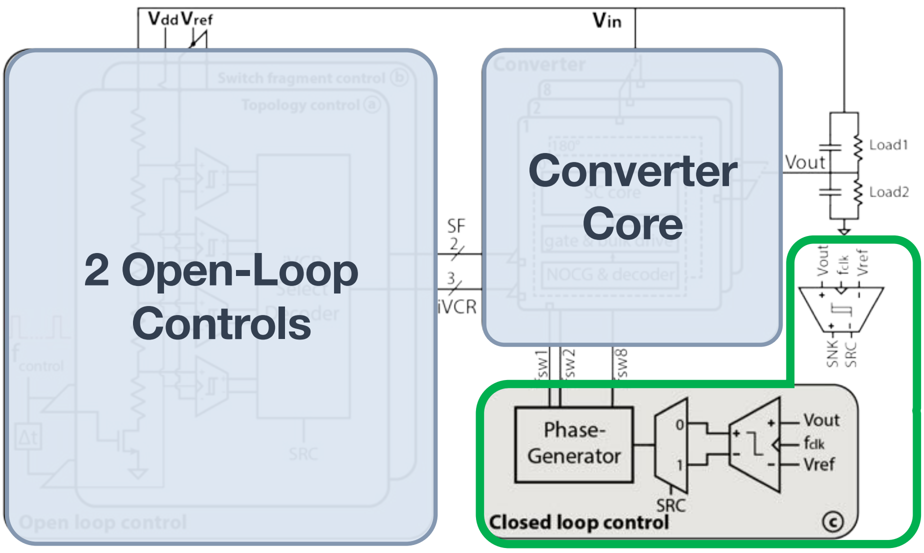
# Toplevel Architecture

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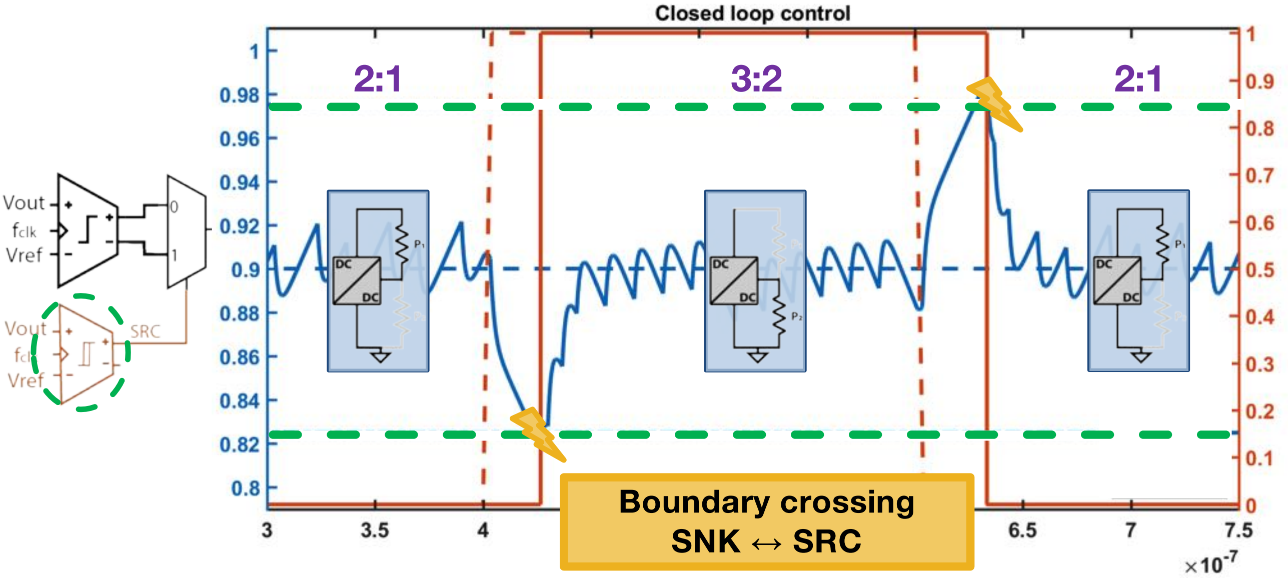
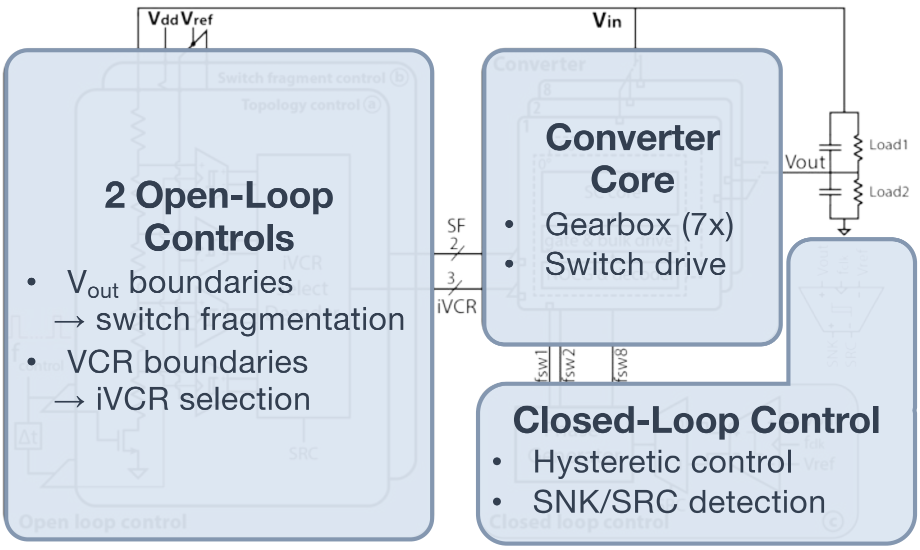
# Closed-Loop Control



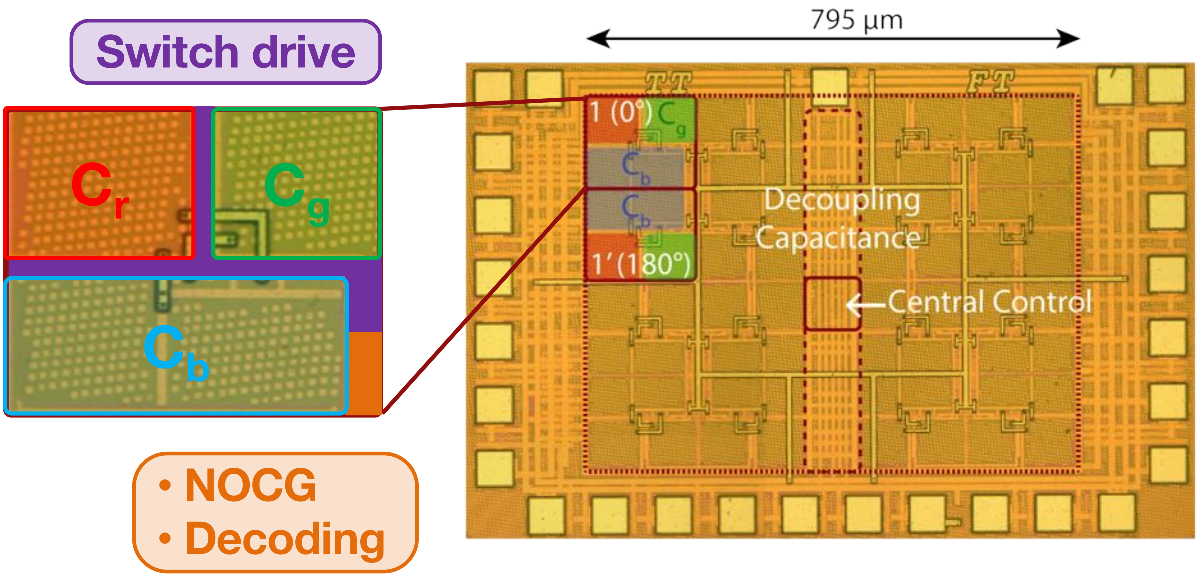

[18] 49

# Toplevel Architecture



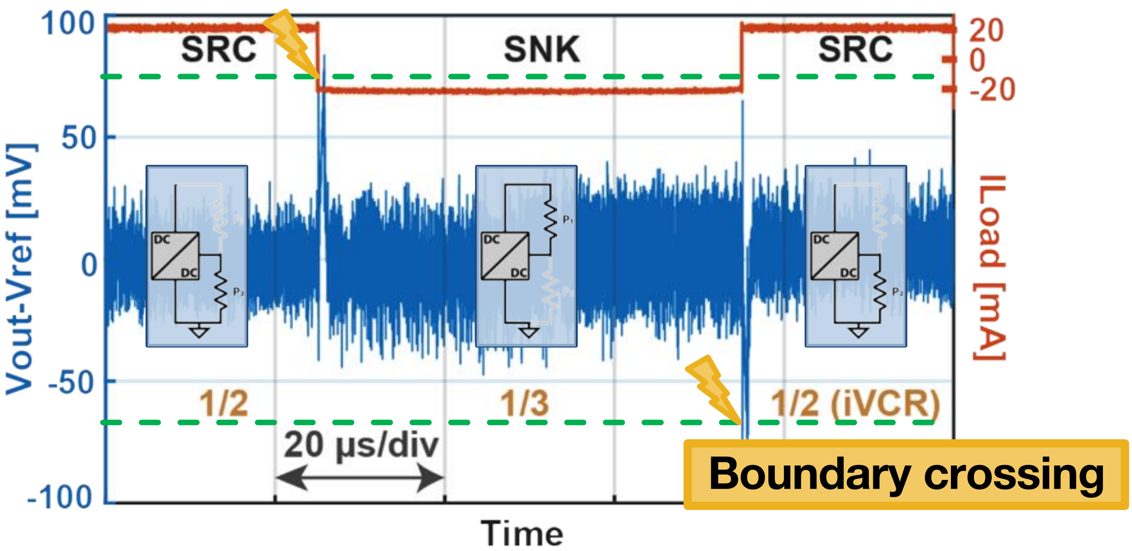

[18] 50

# Chip Micrograph



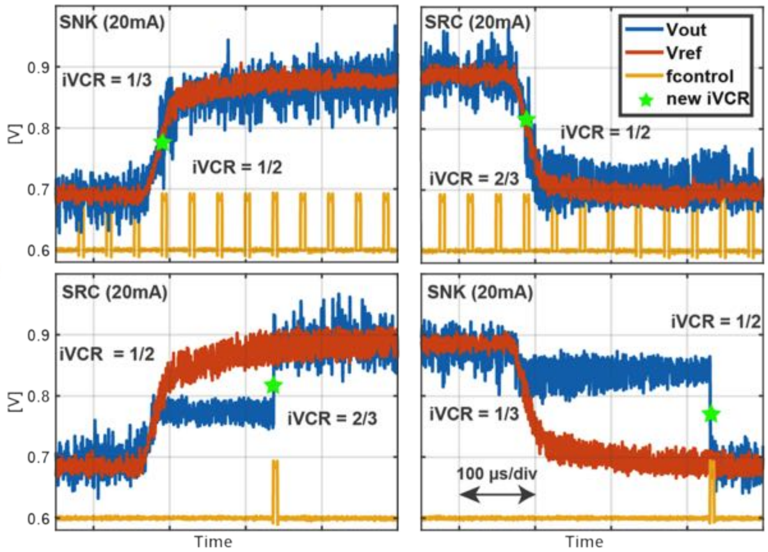

[18] 51

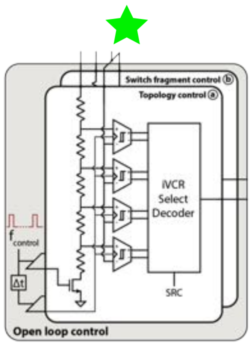
# Maximal Load Step (+/- 20 mA)




[18] 52

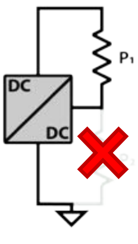
# Open-Loop Control Behaviour

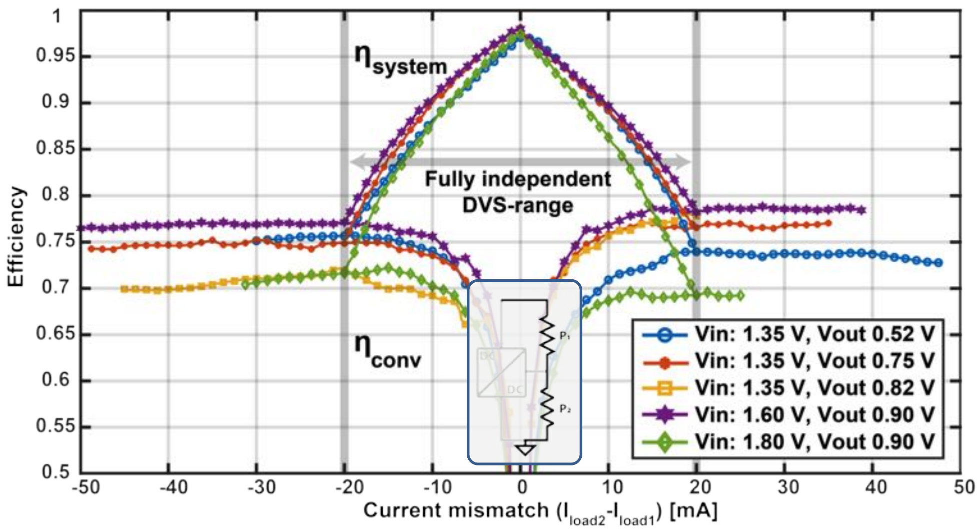


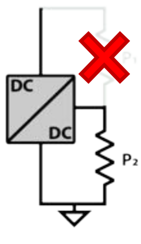




[18] 53

# Efficiency

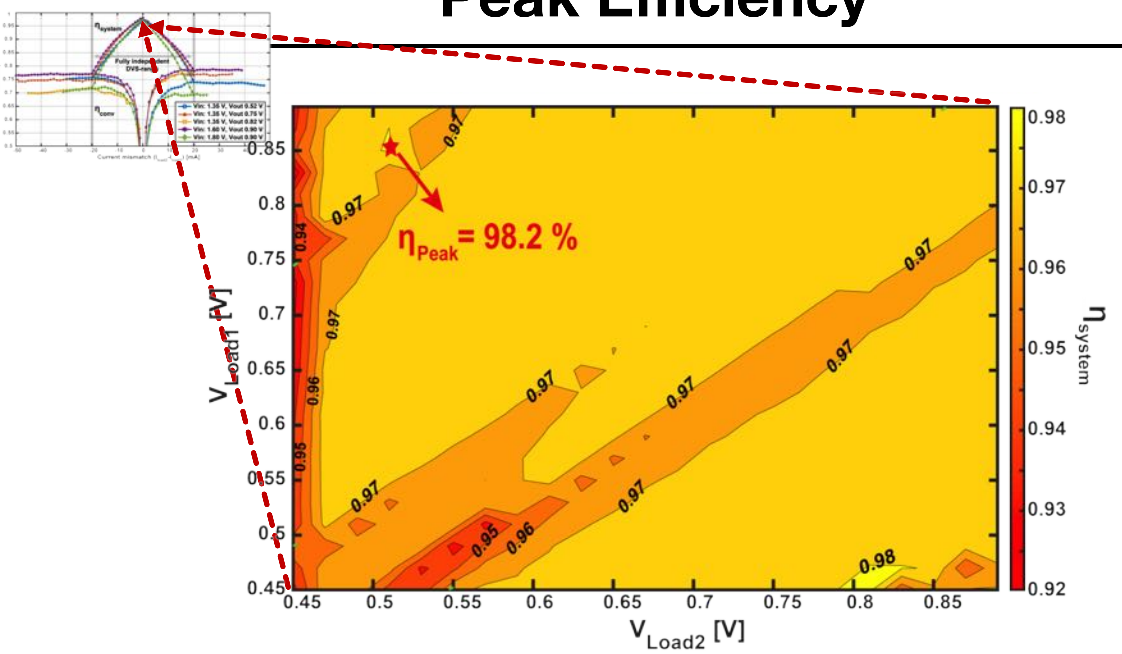



[18] 54

# Peak Efficiency




[18]

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# State-of-the-Art Comparison

| | VDS + DVS | | VDS | | | DVS | |
|---|---|---|---|---|---|---|---|
| | **This work[18]** | **[16]** | **[19]** | **[17]** | **[20]** | **[21]** | **[11]** |
| Technology | **40nm** | 65nm | 40nm | 40nm | 45nm SOI | 65nm LL | 130nm |
| Capacitors | **MOM-MOS** | MOM-MIM | N/A | MOS | Deep-Trench | MOS-MOM-MIM | Ferro-electric |
| DVS-range | **1** | 0.46 | 0 | 0 | 0 | 1 | 1.75 |
| $\delta I_{max}$ | **100%** | 100% | N/A | 15.7% | 60% | / | / |
| $\eta_{peak}$ | **98.2%** | 99.6% | 96% | 99.8% | 99% | 78.3% | 93% |
| $\rho$ [mA/mm$^2$] | **82.64 161.15** | 59.8 140 | 19.09 | / | 4600 | 125 150 | 2.73 |

Widest DVS-range for stacked loads

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# State-of-the-Art Comparison

| | VDS + DVS | | VDS | | | DVS | |
|---|---|---|---|---|---|---|---|
| | **This work[18]** | **[16]** | **[19]** | **[17]** | **[20]** | **[21]** | **[11]** |
| Technology | **40nm** | 65nm | 40nm | 40nm | 45nm SOI | 65nm LL | 130nm |
| Capacitors | **MOM-MOS** | MOM-MIM | N/A | MOS | Deep-Trench | MOS-MOM-MIM | Ferro-electric |
| DVS-range | **1** | 0.46 | 0 | 0 | 0 | 1 | 1.75 |
| $\delta I_{max}$ | **100%** | 100% | N/A | 15.7% | 60% | / | / |
| $\eta_{peak}$ | **98.2%** | 99.6% | 96% | 99.8% | 99% | 78.3% | 93% |
| ρ [mA/mm²] | **82.64 161.15** | 59.8 140 | 19.09 | / | 4600 | 125 150 | 2.73 |

Fully-independent stacked loads

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# State-of-the-Art Comparison

| | VDS + DVS | | VDS | | | DVS | |
|---|---|---|---|---|---|---|---|
| | **This work[18]** | **[16]** | **[19]** | **[17]** | **[20]** | **[21]** | **[11]** |
| Technology | **40nm** | 65nm | 40nm | 40nm | 45nm SOI | 65nm LL | 130nm |
| Capacitors | **MOM-MOS** | MOM-MIM | N/A | MOS | Deep-Trench | MOS-MOM-MIM | Ferro-electric |
| DVS-range | **1** | 0.46 | 0 | 0 | 0 | 1 | 1.75 |
| $\delta I_{max}$ | **100%** | 100% | N/A | 15.7% | 60% | / | / |
| $\eta_{peak}$ | **98.2%** | 99.6% | 96% | 99.8% | 99% | 78.3% | 93% |
| ρ [mA/mm²] | **82.64 161.15** | 59.8 140 | 19.09 | / | 4600 | 125 150 | 2.73 |


High DVS efficiency

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# State-of-the-Art Comparison

| | VDS + DVS | | VDS | | | DVS | |
|---|---|---|---|---|---|---|---|
| | **This work[18]** | **[16]** | **[19]** | **[17]** | **[20]** | **[21]** | **[11]** |
| Technology | **40nm** | 65nm | 40nm | 40nm | 45nm SOI | 65nm LL | 130nm |
| Capacitors | **MOM-MOS** | MOM-MIM | N/A | MOS | Deep-Trench | MOS-MOM-MIM | Ferro-electric |
| DVS-range | **1** | 0.46 | 0 | 0 | 0 | 1 | 1.75 |
| $\delta I_{max}$ | **100%** | 100% | N/A | 15.7% | 60% | / | / |
| $\eta_{peak}$ | **98.2%** | 99.6% | 96% | 99.8% | 99% | 78.3% | 93% |
| ρ [mA/mm²] | **82.64<br>161.15** | 59.8<br>140 | 19.09 | / | 4600 | 125<br>150 | 2.73 |

Highest bulk CMOS current density

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# Outline

- Introduction
- Switched-Capacitor Converters
- Improvements for Energy Storage
- Design Example with Measurements
- **Conclusions**

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# Conclusions

- Autonomous sensor nodes require **energy storage**
- Voltage conversions: harvester ↔ storage ↔ load
- Monolithic and efficient? → **SC Converters**
- VDS limits conversion losses
  - Inherent voltage division → **Lower conversion step**
  - **Lowly loaded** bidirectional unbalance converter
  - Level shifters to communicate between layers
- DVS increases overall power efficiency

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A Capacitive DC-DC Converter for Stacked Loads With Wide Range DVS Achieving 98.2% Peak Efficiency in 40nm CMOS

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